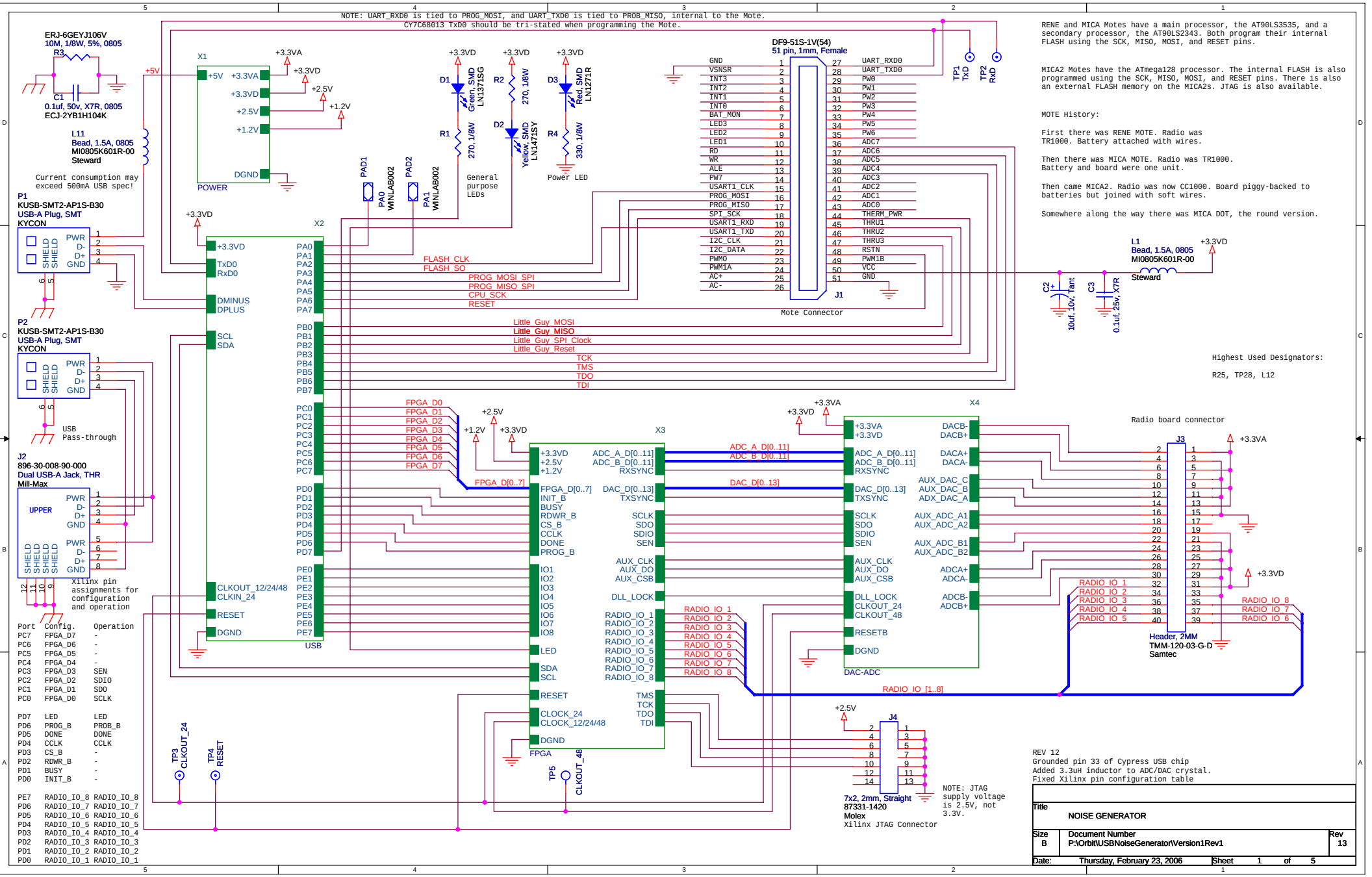
NOTE: UART_RXD0 is tied to PROG_MOSI, and UART_TXD0 is tied to PROB_MISO, internal to the Mote.
CY7C68013 TxD0 should be tri-stated when programming the Mote.
ERJ-6GEYJ106V
10M, 1/8W, 5%, 0805
R3
C1
0.1uf, 50v, X7R, 0805
ECJ-2YB1H104K
L11
Bead, 1.5A, 0805
MI0805K601R-00
Steward
Current consumption may exceed 500mA USB spec!
P1
KUSB-SMT2-AP1S-B30
USB-A Plug, SMT
KYCON
P2
KUSB-SMT2-AP1S-B30
USB-A Plug, SMT
KYCON
USB Pass-through
J2
896-30-008-90-000
Dual USB-A Jack, THR
Mill-Max
UPPER
Xilinx pin assignments for configuration and operation
Port Config. Operation
PC7 FPGA_D7 -
PC6 FPGA_D6 -
PC5 FPGA_D5 -
PC4 FPGA_D4 -
PC3 FPGA_D3 SEN
PC2 FPGA_D2 SDIO
PC1 FPGA_D1 SDO
PC0 FPGA_D0 SCLK
PD7 LED LED
PD6 PROG_B PROB_B
PD5 DONE DONE
PD4 CCLK CCLK
PD3 CS_B -
PD2 RDWR_B -
PD1 BUSY -
PD0 INIT_B -
PE7 RADIO_IO_8 RADIO_IO_8
PE6 RADIO_IO_7 RADIO_IO_7
PE5 RADIO_IO_6 RADIO_IO_6
PE4 RADIO_IO_5 RADIO_IO_5
PE3 RADIO_IO_4 RADIO_IO_4
PE2 RADIO_IO_3 RADIO_IO_3
PE1 RADIO_IO_2 RADIO_IO_2
PE0 RADIO_IO_1 RADIO_IO_1
X1
POWER
+5V
+3.3VA
+3.3VD
+2.5V
+1.2V
DGND
D1 Green, SMD LN1371SG
D2 Yellow, SMD LN1471SY
D3 Red, SMD LN1271R
R1 270, 1/8W
R2 270, 1/8W
R4 330, 1/8W
General purpose LEDs
Power LED
PAD1 PA0 WINLAB002
PAD2 PA1 WINLAB002
X2
USB
TxD0
RxD0
DMINUS
DPLUS
SCL
SDA
CLKOUT_12/24/48
CLKIN_24
RESET
DF9-51S-1V(54)
51 pin, 1mm, Female
J1
Mote Connector
GND VSNSR INT3 INT2 INT1 INT0 BAT_MON LED3 LED2 LED1 RD WR ALE PW7 USART1_CLK PROG_MOSI PROG_MISO SPI_SCK USART1_RXD USART1_TXD I2C_CLK I2C_DATA PWM0 PWM1A AC+ AC-
UART_RXD0 UART_TXD0 PW0 PW1 PW2 PW3 PW4 PW5 PW6 ADC7 ADC6 ADC5 ADC4 ADC3 ADC2 ADC1 ADC0 THERM_PWR THRU1 THRU2 THRU3 RSTN PWM1B VCC GND
TP1 TxD
TP2 RxD
FLASH_CLK
FLASH_SO
PROG_MOSI_SPI
PROG_MISO_SPI
CPU_SCK
RESET
Little_Guy_MOSI
Little_Guy_MISO
Little_Guy_SPI_Clock
Little_Guy_Reset
TCK
TMS
TDO
TDI
L1
Bead, 1.5A, 0805
MI0805K601R-00
Steward
C2 10uf, 10v, Tant
C3 0.1uf, 25v, X7R
RENE and MICA Motes have a main processor, the AT90LS3535, and a secondary processor, the AT90LS2343. Both program their internal FLASH using the SCK, MISO, MOSI, and RESET pins.
MICA2 Motes have the ATmega128 processor. The internal FLASH is also programmed using the SCK, MISO, MOSI, and RESET pins. There is also an external FLASH memory on the MICA2s. JTAG is also available.
MOTE History:
First there was RENE MOTE. Radio was TR1000. Battery attached with wires.
Then there was MICA MOTE. Radio was TR1000. Battery and board were one unit.
Then came MICA2. Radio was now CC1000. Board piggy-backed to batteries but joined with soft wires.
Somewhere along the way there was MICA DOT, the round version.
Highest Used Designators:
R25, TP28, L12
X3
FPGA
FPGA_D0 FPGA_D1 FPGA_D2 FPGA_D3 FPGA_D4 FPGA_D5 FPGA_D6 FPGA_D7
FPGA_D[0..7]
ADC_A_D[0..11]
ADC_B_D[0..11]
DAC_D[0..13]
RXSYNC
TXSYNC
SCLK
SDO
SDIO
SEN
AUX_CLK
AUX_DO
AUX_CSB
DLL_LOCK
RADIO_IO_1 RADIO_IO_2 RADIO_IO_3 RADIO_IO_4 RADIO_IO_5 RADIO_IO_6 RADIO_IO_7 RADIO_IO_8
LED
SDA
SCL
RESET
CLOCK_24
CLOCK_12/24/48
DGND
TMS
TCK
TDO
TDI
X4
DAC-ADC
DACB-
DACB+
DACA+
DACA-
AUX_DAC_C
AUX_DAC_B
ADX_DAC_A
AUX_ADC_A1
AUX_ADC_A2
AUX_ADC_B1
AUX_ADC_B2
ADCA+
ADCA-
ADCB-
ADCB+
RESETB
CLKOUT_24
CLKOUT_48
RADIO_IO_[1..8]
Radio board connector
J3
Header, 2MM
TMM-120-03-G-D
Samtec
J4
7x2, 2mm, Straight
87331-1420
Molex
Xilinx JTAG Connector
NOTE: JTAG supply voltage is 2.5V, not 3.3V.
TP3 CLKOUT_24
TP4 RESET
TP5 CLKOUT_48
REV 12
Grounded pin 33 of Cypress USB chip
Added 3.3uH inductor to ADC/DAC crystal.
Fixed Xilinx pin configuration table
Title
NOISE GENERATOR
Size B
Document Number P:\Orbit\USBNoiseGenerator\Version1Rev1
Rev 13
Date: Thursday, February 23, 2006
Sheet 1 of 5