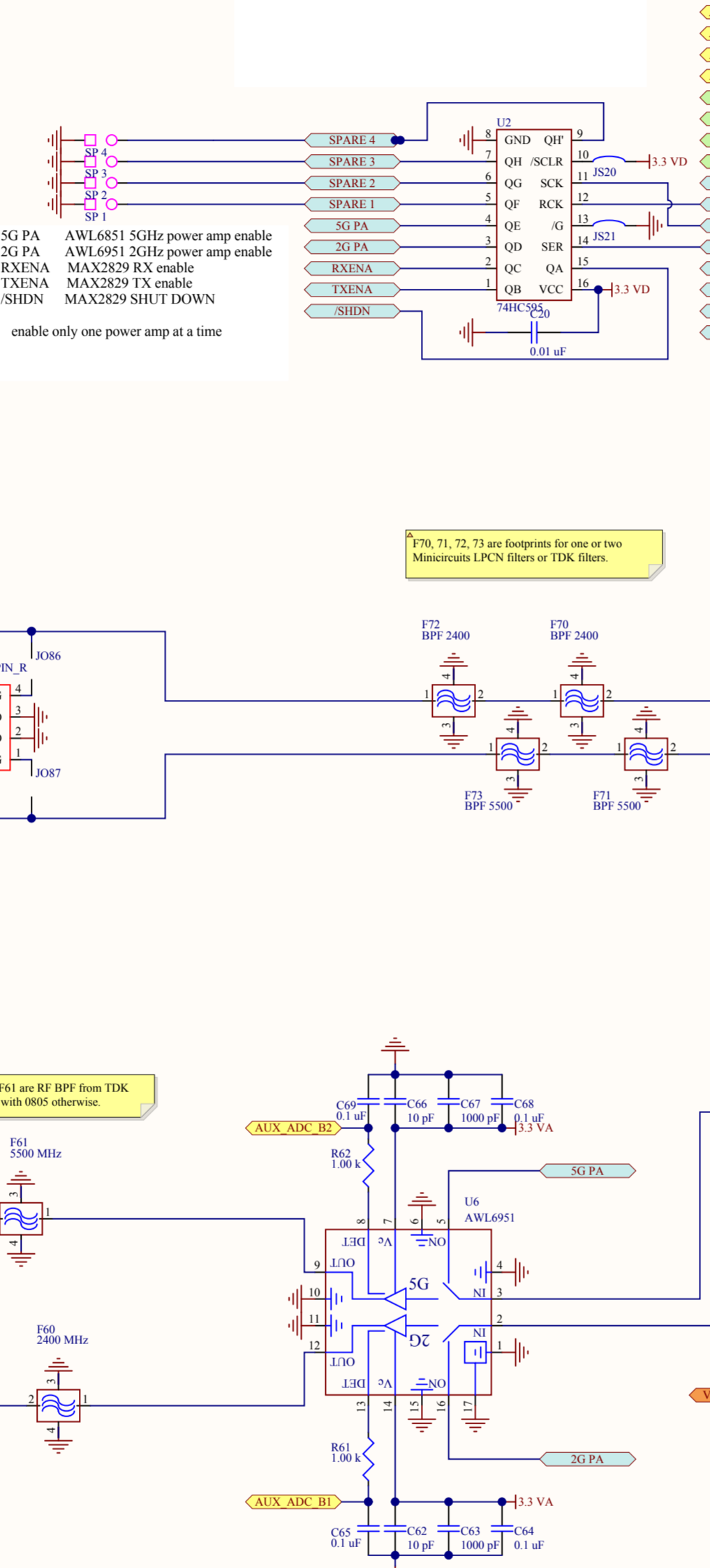


As shown in schematic, four antennas have min. coupling between antennas and freq. bands. Antennas can be arranged at angle for polarization.

JO80, 81, 82, 83 (use C82, 83, 84, 85) give optimal antenna diversity when used in conjunction with U2. enables TX and RX to share one antenna yet still have max spatial diversity (i.e. A01 and A04)



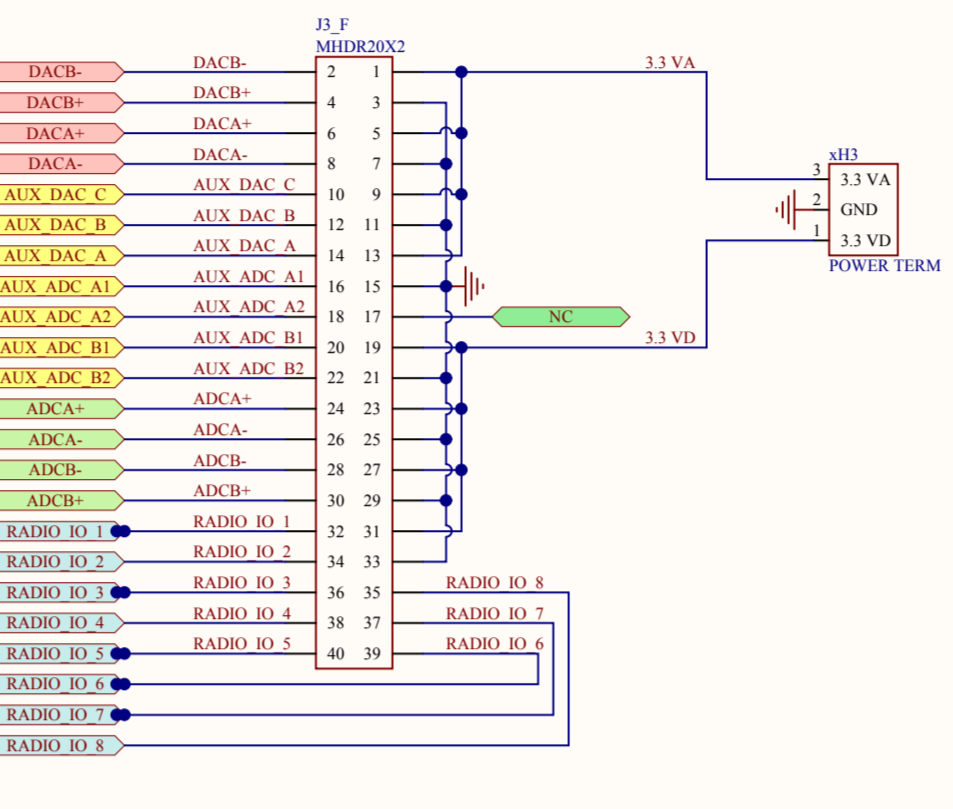
JO80, 81, 82, 83 are extra pads to switch to D01 DIPLEXER\_SPN\_R. use C80, 81 to jumper JO80, 81

F60, F61 are RF BFF from TDK short with 0805 otherwise.

F70, 71, 72, 73 are footprints for one or two Microsemi LPCN filters or TDK filters.

enable only one power amp at a time

- DACB- HI SPD DAC TX Q-
- DACB+ HI SPD DAC TX Q+
- DACA+ HI SPD DAC TX I+
- DACA- HI SPD DAC TX I-
- AUX\_DAC\_C phase modulation of U23
- AUX\_DAC\_B VCXO freq adjust of U9 (when using VC-FXO-45F)
- AUX\_DAC\_A PLL speedup at MAX2829
- AUX\_ADC\_A1 I/2 supply voltage
- AUX\_ADC\_A2 RSSI from MAX2829
- AUX\_ADC\_B1 2G power detector of AWL6951
- AUX\_ADC\_B2 5G power detector of AWL6951
- ADCA+ HI SPD ADC RX I+
- ADCA- HI SPD ADC RX I-
- ADCB+ HI SPD ADC RX Q+
- ADCB- HI SPD ADC RX Q-
- RADIO\_IO\_1 MAX2829\_CS (output)
- RADIO\_IO\_2 U2 RCK (output)
- RADIO\_IO\_3 MAX2829\_SCLK and U2 SCK (output)
- RADIO\_IO\_4 MAX2829\_DIN and U2 SER (output)
- RADIO\_IO\_5 U3 switch (0 = straight, 1 = cross) (output)
- RADIO\_IO\_6 U4 switch (0 = straight, 1 = cross) (output)
- RADIO\_IO\_7 U5 switch (0 = straight, 1 = cross) (output)
- RADIO\_IO\_8 LD (lock detect = 1 = LED ON) (input)



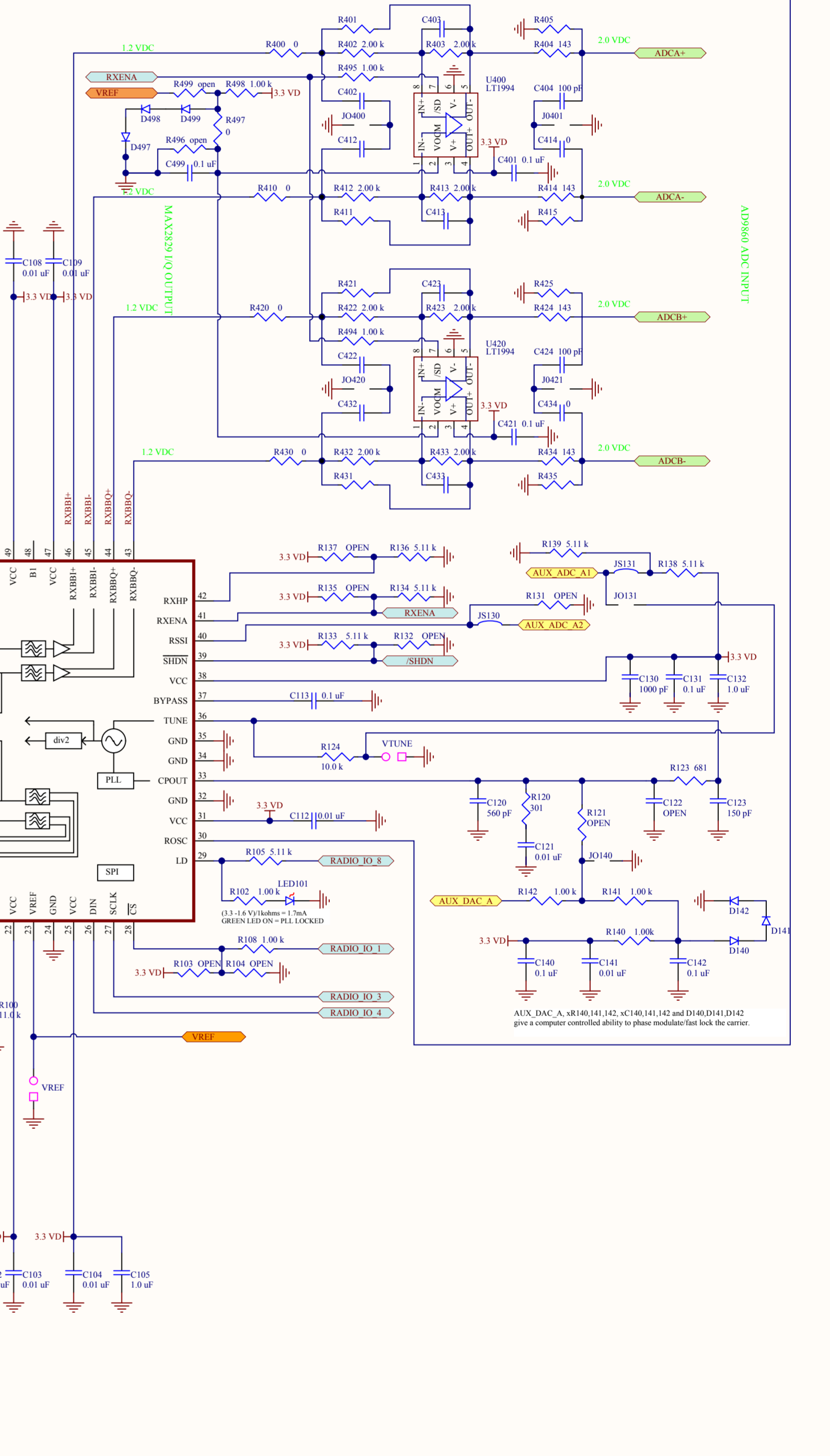
POWERAMP

AUX\_DAC\_B, AWL6951 5GHz power amp enable  
 AUX\_DAC\_C, AWL6951 5GHz power amp enable  
 VCXO freq adjust of U9 (when using VC-FXO-45F)  
 PLL speedup at MAX2829

VCXO spec:  
 Vc = 1.65 ± 1.5V, f = 800MHz  
 VCXO measured result:  
 f(AUX\_DAC\_B) F010  
 8.1 39.9947782 ± 0.3  
 3.0 39.999524  
 Δf = 3.0 Δf = 105.1500Hz/volt, ±100MHz @ 5.6 GHz

FREQ. REF

opt. PHASE ADJ.



TRANSCEIVER

ANTENNA/CONNECTOR

SWITCHES

FILTER/DIPLEXER

Title		
WiBo102		
Size	Number	Revision
Creed D		
Date: 6/6/2006		Sheet of
File: C:\FETS\WINLAB\WiBo102\WBO102.Sch		Drawn By: